**Pipelining Lecture Assignment**

**Dr. Abraham**

1. **Name** Pipe 5 Stages for MIPS -

Define Throughput -

define Machine cycle -

define Stall -

How is Time per instruction on a pipelined computer calculated?

1. If an unpipelined processor has a 1 ns clock cycle and that it uses:

4 cycles for ALU operation and branches

5 cycles for memory operations .

Their relative frequencies are: 40% ALU operations, 20% Branch, and 40% for Memory.

What is the average instruction execution time?

1. If you were to pipeline this processor, one instruction should be completed each cycle (ignoring filling at start and emptying pipeline at the end). Pipelining adds and overhead of .2ns for various things such as latching. So effective time it takes for one instruction is 1.2 ns. What is the speed up gained by pipelining?
2. Name and explain pipeline hazards.
3. Explain the purpose of data forwarding.
4. Explain RAW, WAR and WAW data hazards.