**Chapter 5 review**

**MULTIPLE CHOICE**

1. Which properties do all semiconductor memory cells share?
2. they exhibit two stable states which can be used to represent binary 1 and 0
3. they are capable of being written into to set the state
4. they are capable of being read to sense the state
5. all of the above
6. One distinguishing characteristic of memory that is designated as \_\_\_\_\_\_\_\_\_ is that it is possible to both read data from the memory and to write new data into the memory easily and rapidly.

A. RAM B. ROM

C. EPROM D. EEPROM

1. Which of the following memory types are nonvolatile?

A. erasable PROM B. programmable ROM

C. flash memory D. all of the above

1. In a \_\_\_\_\_\_\_\_\_, binary values are stored using traditional flip-flop logic-gate configurations.

A. ROM B. SRAM

C. DRAM D. RAM

1. A \_\_\_\_\_\_\_\_\_\_ contains a permanent pattern of data that cannot be changed, is nonvolatile, and cannot have new data written into it.

A. RAM B. SRAM

C. ROM D. flash memory

1. With \_\_\_\_\_\_\_\_\_ the microchip is organized so that a section of memory cells are erased in a single action.

A. flash memory B. SDRAM

C. DRAM D. EEPROM

1. \_\_\_\_\_\_\_\_\_\_ can be caused by harsh environmental abuse, manufacturing defects, and wear.

A. SEC errors B. Hard errors

C. Syndrome errors D. Soft errors

1. \_\_\_\_\_\_\_\_\_ can be caused by power supply problems or alpha particles.

A. Soft errors B. AGT errors

C. Hard errors D. SEC errors

1. The \_\_\_\_\_\_\_\_\_ exchanges data with the processor synchronized to an external clock signal and running at the full speed of the processor/memory bus without imposing wait states.

A. DDR-DRAM B. SDRAM

C. CDRAM D. none of the above

1. With \_\_\_\_\_\_\_\_\_\_ the data transfer is synchronized to both the rising and falling edge of the clock, rather than just the rising edge.

A. CDRAM B. SDRAM

C. DDR-DRAM D. RDRAM

1. \_\_\_\_\_\_\_\_\_\_ increases the data transfer rate by increasing the operational frequency of the RAM chip and by increasing the prefetch buffer from 2 bits to 4 bits per chip.

A. DDR2 B. RDRAM

C. CDRAM D. DDR3

1. \_\_\_\_\_\_\_\_ increases the prefetch buffer size to 8 bits.

A. CDRAM B. RDRAM

C. DDR3 D. all of the above

1. Theoretically, a DDR module can transfer data at a clock rate in the range of \_\_\_\_\_\_\_\_\_\_ Mbps.

A. 200 to 400 B. 400 to 1066

C. 600 to 1400 D. 800 to 1600

1. A DDR3 module transfers data at a clock rate of \_\_\_\_\_\_\_\_\_\_ Mbps.

A. 600 to 1200 B. 800 to 2133

C. 1000 to 2000 D. 1500 to 3000

1. \_\_\_\_\_\_\_\_\_\_ is a good candidate to replace or supplement DRAM for main memory.

A. STT-RAM B. ReRAM

C. RamBus D. PCRAM

**SHORT ANSWER**

1. In earlier computers the most common form of random-access storage for computer main memory employed an array of doughnut-shaped ferromagnetic loops referred to as \_\_\_\_\_\_\_\_\_\_.
2. RAM, ROM, PROM, EPROM, EEPROM, and flash memory are all examples of \_\_\_\_\_\_\_\_\_\_ memory types.
3. A \_\_\_\_\_\_\_\_\_ RAM is made with cells that store data as charge on capacitors.
4. A \_\_\_\_\_\_\_\_\_\_ RAM is a digital device that uses the same logic elements used in the processor.
5. Three common forms of read-mostly memory are: EPROM, EEPROM, and \_\_\_\_\_\_\_\_\_.
6. A \_\_\_\_\_\_\_\_\_\_ failure is a permanent physical defect so that the memory cell or cells affected cannot reliably store data but become stuck at 0 or 1 or switch erratically between 0 and 1.
7. A \_\_\_\_\_\_\_\_\_\_ error is a random, nondestructive event that alters the contents of one or more memory cells without damaging the memory.
8. The simplest of the error-correcting codes is the \_\_\_\_\_\_\_\_\_ code.
9. One of the most widely used forms of DRAM is the \_\_\_\_\_\_\_\_\_ DRAM.
10. The two distinctive types of flash memory are designated as NOR and \_\_\_\_\_\_ .
11. \_\_\_\_\_\_\_\_\_\_\_ is a new type of Magnetic RAM, which features non-volatility, fast writing/reading speed, and high programming endurance and zero standby power.
12. \_\_\_\_\_\_\_\_\_\_ works by creating resistance rather than directly storing charge.
13. A new version of SDRAM, referred to as \_\_\_\_\_\_\_\_\_\_, can send data twice per clock cycle, once on the rising edge of the clock pulse and once on the falling edge.
14. The traditional \_\_\_\_\_\_\_\_\_\_ chip is constrained both by its internal architecture and by its interface to the processor’s memory bus.
15. A typical DRAM pin configuration will include the \_\_\_\_\_\_\_\_\_\_ pin if necessary in order to have an even number of pins.