**Chapter 4: CACHE MEMORY**

**MULTIPLE CHOICE**

1. \_\_\_\_\_\_\_\_\_\_ refers to whether memory is internal or external to the computer.

A. Location B. Access

C. Hierarchy D. Tag

1. Internal memory capacity is typically expressed in terms of \_\_\_\_\_\_\_\_\_.

A. hertz B. nanos

C. bytes D. LOR

1. For internal memory, the \_\_\_\_\_\_\_\_\_\_ is equal to the number of electrical lines into and out of the memory module.

A. access time B. unit of transfer

C. capacity D. memory ratio

1. “Memory is organized into records and access must be made in a specific linear sequence” is a description of \_\_\_\_\_\_\_\_\_\_.

A. sequential access B. direct access

C. random access D. associative access

1. individual blocks or records have a unique address based on physical location with \_\_\_\_\_\_\_\_\_\_.

A. associative access B. physical access

C. direct access D. sequential access

1. For random-access memory, \_\_\_\_\_\_\_\_\_\_ is the time from the instant that an address is presented to the memory to the instant that data have been stored or made available for use.

A. memory cycle time B. direct access

C. transfer rate D. access time

1. The \_\_\_\_\_\_\_\_ consists of the access time plus any additional time required before a second access can commence.

A. latency B. memory cycle time

C. direct access D. transfer rate

1. A portion of main memory used as a buffer to hold data temporarily that is to be read out to disk is referred to as a \_\_\_\_\_\_\_\_\_.

A. disk cache B. latency

C. virtual address D. miss

1. A line includes a \_\_\_\_\_\_\_\_\_ that identifies which particular block is currently being stored.

A. cache B. hit

C. tag D. locality

1. \_\_\_\_\_\_\_\_\_\_ is the simplest mapping technique and maps each block of main memory into only one possible cache line.

A. Direct mapping B. Associative mapping

C. Set associative mapping D. None of the above

1. When using the \_\_\_\_\_\_\_\_\_\_ technique all write operations made to main memory are made to the cache as well.

A. write back B. LRU

C. write through D. unified cache

1. The key advantage of the \_\_\_\_\_\_\_\_\_\_ design is that it eliminates contention for the cache between the instruction fetch/decode unit and the execution unit.

A. logical cache B. split cache

C. unified cache D. physical cache

1. The Pentium 4 \_\_\_\_\_\_\_\_\_ component executes micro-operations, fetching the required data from the L1 data cache and temporarily storing results in registers.

A. fetch/decode unit B. out-of-order execution logic

C. execution unit D. memory subsystem

1. In reference to access time to a two-level memory, a \_\_\_\_\_\_\_\_\_ occurs if an accessed word is not found in the faster memory.

A. miss B. hit

C. line D. tag

1. A logical cache stores data using \_\_\_\_\_\_\_\_\_\_.

A. physical addresses B. virtual addresses

C. random addresses D. none of the above

**SHORT ANSWER**

1. \_\_\_\_\_\_\_\_\_\_ memory consists of peripheral storage devices, such as disk and tape.
2. One byte equals \_\_\_\_\_\_\_\_\_\_ bits.
3. From a user’s point of view the two most important characteristics of memory are capacity and \_\_\_\_\_\_\_\_\_\_\_\_\_.
4. The three performance parameters for memory are: access time, transfer rate, and \_\_\_\_\_\_\_\_\_.
5. \_\_\_\_\_\_\_\_\_ is a random access type of memory that enables one to make a comparison of desired bit locations within a word for a specified match, and to do this for all words simultaneously, thus retrieving a word based on a portion of its contents rather than its address.
6. The \_\_\_\_\_\_\_\_ rate is the rate at which data can be transferred into or out of a memory unit.
7. The most commonly used physical types of memory are: semiconductor memory, \_\_\_\_\_\_\_\_\_\_ memory (used for disk and tape), and optical and magneto-optical.
8. The three key characteristics of memory are capacity, access time, and \_\_\_\_\_\_\_.
9. External, nonvolatile memory is referred to as \_\_\_\_\_\_\_\_\_\_\_ or auxiliary memory.
10. The cache consists of blocks called \_\_\_\_\_\_\_\_\_\_.
11. \_\_\_\_\_\_\_\_\_\_ computing deals with super computers and their software.
12. The Pentium 4 processor core consists of four major components: fetch/decode unit, out-of-order execution logic, memory subsystem, and \_\_\_\_\_\_\_\_\_\_.
13. The \_\_\_\_\_\_\_\_\_\_ units execute micro-operations, fetching the required data from the L1 data cache and temporarily storing results in registers.
14. \_\_\_\_\_\_\_\_\_\_ memory is a facility that allows programs to address memory from a logical point of view, without regard to the amount of main memory physically available.
15. For set-associative mapping the cache control logic interprets a memory address as three fields: Set, Word, and \_\_\_\_\_\_\_\_\_\_.