**Chapter 15: reduced instruction set computers**

**MULTIPLE CHOICE**

1. \_\_\_\_\_\_\_\_\_ determines the control and pipeline organization.

A. Calculation B. Execution sequencing

C. Operations performed D. Operands used

1. The Patterson study examined the dynamic behavior of \_\_\_\_\_\_\_\_\_ programs, independent of the underlying architecture.

A. HLL B. RISC

C. CISC D. all of the above

1. \_\_\_\_\_\_\_\_\_ is the fastest available storage device.

A. Main memory B. Cache

C. Register storage D. HLL

1. The first commercial RISC product was \_\_\_\_\_\_\_\_\_.

A. SPARC B. CISC

C. VAX D. the Pyramid

1. \_\_\_\_\_\_\_\_\_ instructions are used to position quantities in registers temporarily for computational operations.

A. Load-and-store B. Window

C. Complex D. Branch

1. Which stage is required for load and store operations?

A. I B. E

C. D D. all of the above

1. A \_\_\_\_\_\_\_\_ instruction can be used to account for data and branch delays.

A. SUB B. NOOP

C. JUMP D. all of the above

1. The instruction location immediately following the delayed branch is referred to as the \_\_\_\_\_\_\_\_.

A. delay load B. delay file

C. delay slot D. delay register

1. A tactic similar to the delayed branch is the \_\_\_\_\_\_\_\_\_, which can be used on LOAD instructions.

A. delayed load B. delayed program

C. delayed slot D. delayed register

1. The MIPS R4000 uses \_\_\_\_\_\_\_\_ bits for all internal and external data paths and for addresses, registers, and the ALU.

A. 16 B. 32

C. 64 D. 128

1. All MIPS R series processor instructions are encoded in a single \_\_\_\_\_\_\_\_ word format.

A. 4-bit B. 8-bit

C. 16-bit D. 32-bit

1. A \_\_\_\_\_\_\_\_\_ architecture is one that makes use of more, and more fine-grained pipeline stages.

A. parallel B. superpipelined

C. superscalar D. hybrid

1. The R4000 can have as many as \_\_\_\_\_\_\_ instructions in the pipeline at the same time.

A. 8 B. 10

C. 5 D. 3

1. SPARC refers to an architecture defined by \_\_\_\_\_\_\_\_.

A. Microsoft B. Apple

C. Sun Microsystems D. IBM

1. The R4000 pipeline stage where the instruction result is written back to the register file is the \_\_\_\_\_\_\_\_\_\_ stage.

A. write back B. tag check

C. data cache D. instruction execute

**SHORT ANSWER**

1. Introduced by IBM with its System/360, the \_\_\_\_\_\_\_\_\_ is a set of computers offered with different price and performance characteristics that presents the same architecture to the user.
2. A large number of general-purpose registers, and/or the use of compiler technology to optimize register usage, a limited and simple instruction set, and an emphasis on optimizing the instruction pipeline are all key elements of \_\_\_\_\_\_\_\_\_ architectures.
3. The difference between the operations provided in high-level languages (HLLs) and those provided in computer architecture is known as the \_\_\_\_\_\_\_\_.
4. Blocks of memory, recently used global variables, memory addressing, and one operand addressed and accessed per cycle are characteristics of \_\_\_\_\_\_\_\_\_ organizations.
5. Individual variables, compiler assigned global variables, register addressing, and multiple operands addressed and accessed in one cycle are characteristics of \_\_\_\_\_\_\_\_\_\_ organizations.
6. The acronym RISC stands for \_\_\_\_\_\_\_\_\_\_.
7. Although a variety of different approaches to reduced instruction set architecture have been taken, certain characteristics are common to all of them: register-to-register operations, simple addressing modes, simple instruction formats, and \_\_\_\_\_\_\_\_\_\_.
8. A \_\_\_\_\_\_\_\_ is defined to be the time it takes to fetch two operands from registers, perform an ALU operation, and store the result in a register.
9. The acronym CISC stands for \_\_\_\_\_\_\_\_\_.
10. \_\_\_\_\_\_\_\_\_\_ is a way of increasing the efficiency of the pipeline by making use of a branch that does not take effect until after execution of the following instruction.
11. \_\_\_\_\_\_\_\_ can improve performance by reducing loop overhead, increasing instruction parallelism by improving pipeline performance, and improving register, data cache, or TLB locality.
12. The MIPS R4000 processor chip is partitioned into two sections, one containing the CPU and the other containing a \_\_\_\_\_\_\_\_\_ for memory management.
13. A \_\_\_\_\_\_\_\_ architecture replicates each of the pipeline stages so that two or more instructions at the same stage of the pipeline can be processed simultaneously.
14. The acronym SPARC stands for \_\_\_\_\_\_\_\_\_\_.
15. The work that has been done on assessing merits of the RISC approach can be grouped into two categories: quantitative and \_\_\_\_\_\_\_\_\_.