**Chapter 14: processor structure and function**

**MULTIPLE CHOICE**

1. \_\_\_\_\_\_\_\_\_\_ are a set of storage locations.

A. Processors B. PSWs

C. Registers D. Control units

1. The \_\_\_\_\_\_\_\_ controls the movement of data and instructions into and out of the processor.

A. control unit B. ALU

C. shifter D. branch

1. \_\_\_\_\_\_\_\_ registers may be used only to hold data and cannot be employed in the calculation of an operand address.

A. General purpose B. Data

C. Address D. Condition code

1. \_\_\_\_\_\_\_\_\_\_ are bits set by the processor hardware as the result of operations.

A. MIPS B. Condition codes

C. Stacks D. PSWs

1. The \_\_\_\_\_\_\_\_\_ contains the address of an instruction to be fetched.

A. instruction register B. memory address register

C. memory buffer register D. program counter

1. The \_\_\_\_\_\_\_\_\_ contains a word of data to be written to memory or the word most recently read.

A. MAR B. PC

C. MBR D. IR

1. The \_\_\_\_\_\_\_\_ determines the opcode and the operand specifiers.

A. decode instruction B. fetch operands

C. calculate operands D. execute instruction

1. \_\_\_\_\_\_\_\_\_ is a pipeline hazard.

A. Control B. Resource

C. Data D. All of the above

1. A \_\_\_\_\_\_\_\_ hazard occurs when there is a conflict in the access of an operand location.

A. resource B. data

C. structural D. control

1. A \_\_\_\_\_\_\_\_\_ is a small, very-high-speed memory maintained by the instruction fetch stage of the pipeline and containing the *n* most recently fetched instructions in sequence.

A. loop buffer B. delayed branch

C. multiple stream D. branch prediction

1. The \_\_\_\_\_\_\_\_\_ is a small cache memory associated with the instruction fetch stage of the pipeline.

A. dynamic branch B. loop table

C. branch history table D. flag

1. The \_\_\_\_\_\_\_\_\_ stage includes ALU operations, cache access, and register update.

A. decode B. execute

C. fetch D. write back

1. \_\_\_\_\_\_\_\_ is used for debugging.

A. Direction flag B. Alignment check

C. Trap flag D. Identification flag

1. The ARM architecture supports \_\_\_\_\_\_\_ execution modes.

A. 2 B. 8

C. 11 D. 7

1. The OS usually runs in \_\_\_\_\_\_\_\_.

A. supervisor mode B. abort mode

C. undefined mode D. fast interrupt mode

**SHORT ANSWER**

1. A processor must: fetch instruction, interpret instruction, process data, write data, and \_\_\_\_\_\_\_\_\_.
2. The major components of the processor are an arithmetic and logic unit (ALU) and a \_\_\_\_\_\_\_\_\_\_.
3. The \_\_\_\_\_\_\_\_\_ element is needed to transfer data between the various registers and the ALU.
4. \_\_\_\_\_\_\_\_\_ registers enable the machine or assembly language programmer to minimize main memory references by optimizing use of registers.
5. \_\_\_\_\_\_\_\_\_\_ registers are used by the control unit to control the operation of the processor and by privileged operating system programs to control the execution of programs.
6. Many processor designs include a register or set of registers often known as the \_\_\_\_\_\_\_\_\_ that contain status information and condition codes.
7. An instruction cycle includes the following stages: fetch, execute, and \_\_\_\_\_\_\_.
8. \_\_\_\_\_\_\_\_\_\_ is a process where new inputs are accepted at one end before previously accepted inputs appear as outputs at the other end.
9. \_\_\_\_\_\_\_\_\_\_ or *fetch overlap* is where, while the second stage is executing the instruction, the first stage takes advantage of any unused memory cycles to fetch and buffer the next instruction.
10. A \_\_\_\_\_\_\_\_\_\_ occurs when the pipeline, or some portion of the pipeline, must stall because conditions do not permit continued execution.
11. The three types of data hazards are: read after write (RAW), write after write (WAW), and \_\_\_\_\_\_\_\_\_.
12. A \_\_\_\_\_\_\_\_\_, also known as a *branch hazard,* occurs when the pipeline makes the wrong decision on a branch prediction and therefore brings instructions into the pipeline that must subsequently be discarded.
13. Two classes of events cause the x86 to suspend execution of the current instruction stream and respond to the event: interrupts and \_\_\_\_\_\_\_\_.
14. The \_\_\_\_\_\_\_\_ flag allows the programmer to disable debug exceptions so that the instruction can be restarted after a debug exception without immediately causing another debug exception.
15. Data are exchanged with the processor from external memory through a \_\_\_\_\_\_\_\_\_.