**MULTIPLE CHOICE**

1. The superscalar approach can be used on \_\_\_\_\_\_\_\_\_\_ architecture.

A. RISC B. CISC

C. neither RISC nor CISC D. both RISC and CISC

1. The essence of the \_\_\_\_\_\_\_\_ approach is the ability to execute instructions independently and concurrently in different pipelines.

A. scalar B. branch

C. superscalar D. flow dependency

1. Which of the following is a fundamental limitation to parallelism with which the system must cope?

A. procedural dependency B. resource conflicts

C. antidependency D. all of the above

1. The situation where the second instruction needs data produced by the first instruction to execute is referred to as \_\_\_\_\_\_\_\_\_\_.

A. true data dependency B. output dependency

C. procedural dependency D. antidependency

1. The instructions following a branch have a \_\_\_\_\_\_\_\_\_ on the branch and cannot be executed until the branch is executed.

A. resource dependency B. procedural dependency

C. output dependency D. true data dependency

1. \_\_\_\_\_\_\_\_ refers to the process of initiating instruction execution in the processor’s functional units.

A. Instruction issue B. In-order issue

C. Out-of-order issue D. Procedural issue

1. Instead of the first instruction producing a value that the second instruction uses, with \_\_\_\_\_\_\_\_\_\_\_ the second instruction destroys a value that the first instruction uses.

A. in-order issue B. resource conflict

C. antidependency D. out-of-order completion

1. \_\_\_\_\_\_\_\_ indicates whether this micro-op is scheduled for execution, has been dispatched for execution, or has completed execution and is ready for retirement.

A. State B. Memory address

C. Micro-op D. Alias register

1. \_\_\_\_\_\_\_\_\_\_ exists when instructions in a sequence are independent and thus can be executed in parallel by overlapping.

A. Flow dependency B. Instruction-level parallelism

C. Machine parallelism D. Instruction issue

1. \_\_\_\_\_\_\_\_\_ is determined by the number of instructions that can be fetched and executed at the same time and by the speed and sophistication of the mechanisms that the processor uses to find independent instructions.

A. Machine parallelism B. Instruction-level parallelism

C. Output dependency D. Procedural dependency

1. \_\_\_\_\_\_\_\_ is a protocol used to issue instructions.

A. Micro-ops B. Scalar

C. SIMD D. Instruction issue policy

1. \_\_\_\_\_\_\_\_ is used in scalar RISC processors to improve the performance of instructions that require multiple cycles.

A. In-order completion B. In-order issue

C. Out-of-order completion D. Out-of-order issue

1. Which of the following is a hardware technique that can be used in a superscalar processor to enhance performance?

A. duplication of resources B. out-of-order issue

C. renaming D. all of the above

1. The \_\_\_\_\_\_\_\_ introduced a full-blown superscalar design with out-of-order execution.

A. Pentium B. Pentium Pro

C. 386 D. 486

1. Utilizing a branch target buffer (BTB), the \_\_\_\_\_\_\_\_\_ uses a dynamic branch prediction strategy based on the history of recent executions of branch instructions.

A. 486 B. Pentium

C. Intel Core D. Pentium Pro

**SHORT ANSWER**

1. A \_\_\_\_\_\_\_\_ implementation of a processor architecture is one in which common instructions can be initiated simultaneously and executed independently.
2. The term \_\_\_\_\_\_\_\_ refers to a machine that is designed to improve the performance of the execution of scalar instructions.
3. \_\_\_\_\_\_\_\_ exploits the fact that many pipeline stages perform tasks that require less than half a clock cycle.
4. The term \_\_\_\_\_\_\_\_\_ parallelism refers to the degree to which, on average, the instructions of a program can be executed in parallel.
5. A \_\_\_\_\_\_\_\_\_ is a competition of two or more instructions for the same resource at the same time.
6. \_\_\_\_\_\_\_\_\_ is a measure of the ability of the processor to take advantage of instruction-level parallelism.
7. Committing or \_\_\_\_\_\_\_\_\_ the instruction is when instructions are conceptually put back into sequential order and their results are recorded.
8. In the operation of the Intel Core each instruction is translated into one or more fixed-length RISC instructions known as \_\_\_\_\_\_\_\_\_.
9. The \_\_\_\_\_\_\_\_ protects critical data used by the operating system from user applications, separating processing tasks by disallowing access to each other’s data, disabling access to memory regions, allowing memory regions to be defined as read-only, and detecting unexpected memory accesses that could potentially break the system.
10. The \_\_\_\_\_\_\_\_\_ predicts the instruction stream, fetches instructions from the L1 instruction cache, and places the fetched instructions into a buffer for consumption by the decode pipeline.
11. Instruction-level parallelism is also determined by \_\_\_\_\_\_\_\_\_\_, which is the time until the result of an instruction is available for use as an operand in a subsequent instruction.
12. Superscalar instruction issue policies are grouped into the following categories: in-order issue with in-order completion, out-of-order issue with out-of-order completion, and \_\_\_\_\_\_\_\_\_\_\_\_.
13. With \_\_\_\_\_\_\_\_\_\_\_\_ any number of instructions may be in the execution stage at any one time, up to the maximum degree of machine parallelism across all functional units.
14. The \_\_\_\_\_\_\_\_ is a buffer used to decouple the decode and execute stages of the pipeline to allow out-of-order issue.
15. An alternative to \_\_\_\_\_\_\_\_\_ is a scoreboarding.