**Chapter 3:**

**A Top-Level viEw of Computer Function and INterconnection**

**MULTIPLE CHOICE**

1. Virtually all contemporary computer designs are based on concepts developed by \_\_\_\_\_\_\_\_\_\_ at the Institute for Advanced Studies, Princeton.

A. John Maulchy B. John von Neumann

C. Herman Hollerith D. John Eckert

1. The von Neumann architecture is based on which concept?
2. data and instructions are stored in a single read-write memory
3. the contents of this memory are addressable by location
4. execution occurs in a sequential fashion
5. all of the above
6. A sequence of codes or instructions is called \_\_\_\_\_\_\_\_\_\_.

A. software B. memory

C. an interconnect D. a register

1. The processing required for a single instruction is called a(n) \_\_\_\_\_\_\_\_\_\_ cycle.

A. execute B. fetch

C. instruction D. packet

1. A(n) \_\_\_\_\_\_\_\_\_ is generated by a failure such as power failure or memory parity error.

A. I/O interrupt B. hardware failure interrupt

C. timer interrupt D. program interrupt

1. A(n) \_\_\_\_\_\_\_\_\_ is generated by some condition that occurs as a result of an instruction execution.

A. timer interrupt B. I/O interrupt

C. program interrupt D. hardware failure interrupt

1. The interconnection structure must support which transfer?
2. memory to processor
3. processor to memory
4. I/O to or from memory
5. all of the above
6. A bus that connects major computer components (processor, memory, I/O) is called a \_\_\_\_\_\_\_\_\_\_.

A. system bus B. address bus

C. data bus D. control bus

1. The \_\_\_\_\_\_\_\_\_\_ are used to designate the source or destination of the data on the data bus.

A. system lines B. data lines

C. control lines D. address lines

1. The data lines provide a path for moving data among system modules and are collectively called the \_\_\_\_\_\_\_\_\_.

A. control bus B. address bus

C. data bus D. system bus

1. A \_\_\_\_\_\_\_\_\_\_ is the high-level set of rules for exchanging packets of data between devices.

A. bus B. protocol

C. packet D. QPI

1. Each data path consists of a pair of wires (referred to as a \_\_\_\_\_\_\_\_\_\_ ) that

transmits data one bit at a time*.*

A. lane B. path

C. line D. bus

1. The \_\_\_\_\_\_\_\_\_ receives read and write requests from the software above the TL and creates request packets for transmission to a destination via the link layer.

A. transaction layer B. root layer

C. configuration layer D. transport layer

1. The TL supports which of the following address spaces?
2. memory
3. I/O
4. message
5. all of the above
6. The QPI \_\_\_\_\_\_\_\_\_ layer is used to determine the course that a packet will traverse across the available system interconnects.

A. link B. protocol

C. routing D. physical

**SHORT ANSWER**

1. A \_\_\_\_\_\_\_\_\_\_ register specifies the address in memory for the next read or write.
2. A \_\_\_\_\_\_\_\_\_ register contains the data to be written into memory or receives the data read from memory.
3. The most common classes of interrupts are: program, timer, I/O and \_\_\_\_\_\_\_\_.
4. A(n) \_\_\_\_\_\_\_\_\_ interrupt is generated by a timer within the processor and allows the operating system to perform certain functions on a regular basis.
5. A(n) \_\_\_\_\_\_\_\_ interrupt is generated by an I/O controller to signal normal completion of an operation, request service from the processor, or to signal a variety of error conditions.
6. A \_\_\_\_\_\_\_\_\_ interrupt simply means that the processor can and will ignore that interrupt request signal.
7. The collection of paths connecting the various modules is called the \_\_\_\_\_\_\_\_\_ structure.
8. A \_\_\_\_\_\_\_\_\_\_ is a communication pathway connecting two or more devices.
9. The \_\_\_\_\_\_\_\_\_ lines are used to control the access to and the use of the data and address lines.
10. There are three important groups of DLLPs used in managing a link: flow control packets, ­­­­­­­­­­\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ , and TLP ACK and NAK packets.
11. The purpose of the PCIe \_\_\_\_\_\_\_\_\_\_ layer is to ensure reliable delivery of packets across the PCIe link.
12. With \_\_\_\_\_\_\_\_\_ transmission signals are transmitted as a current that travels down one conductor and returns on the other.
13. The QPI link layer performs two key functions: flow control and \_\_\_\_\_\_\_\_\_ control.
14. The \_\_\_\_\_\_\_\_\_\_ is a popular high-bandwidth, processor-independent bus that can function as a mezzanine or peripheral bus.
15. The \_\_\_\_\_\_\_\_\_ function is needed to ensure that a sending QPI entity does not overwhelm a receiving QPI entity by sending data faster than the receiver can process the data and clear buffers for more incoming data.