**Chapter 18: multicore computers**

**MULTIPLE CHOICE**

1. With \_\_\_\_\_\_\_, register banks are replicated so that multiple threads can share the use of pipeline resources.

A. SMT B. pipelining

C. scalar D. superscalar

1. \_\_\_\_\_\_\_\_\_ is where individual instructions are executed through a pipeline of stages so that while one instruction is executing in one stage of the pipeline, another instruction is executing in another stage of the pipeline.

A. Superscalar B. Scalar

C. Pipelining D. Simultaneous multithreading

1. \_\_\_\_\_\_\_\_\_ is when multiple pipelines are constructed by replicating execution resources, enabling parallel execution of instructions in parallel pipelines so long as hazards are avoided.

A. Vectoring B. Superscalar

C. Hybrid multithreading D. Pipelining

1. One way to control power density is to use more of the chip area for \_\_\_\_\_\_\_\_.

A. multicore B. cache memory

C. silicon D. resistors

1. \_\_\_\_\_\_\_\_\_\_\_ states that performance increase is roughly proportional to square root of increase in complexity.

A. Pollack’s Rule B. Moore’s Law

C. Amdahl’s Law D. MOESI Rule

1. \_\_\_\_\_\_\_\_\_\_ applications are characterized by the presence of many single-threaded processes.

A. Java B. Multithreaded native

C. Multi-instance D. Multiprocess

1. \_\_\_\_\_\_\_ applications embrace threading in a fundamental way.

A. Multi-instance B. Multi-process

C. Java D. Threaded

1. Putting rendering on one processor, AI on another, and physics on another is an example of \_\_\_\_\_\_\_\_\_ threading.

A. coarse-grained B. multi-instance

C. fine-grained D. hybrid

1. A loop that iterates over an array of data can be split up into a number of smaller parallel loops in individual threads that can be scheduled in parallel when using \_\_\_\_\_\_\_\_ threading.

A. multi-process B. fine-grained

C. hybrid D. coarse

1. The \_\_\_\_\_\_\_\_\_ is an example of splitting off a separate, shared L3 cache, with dedicated L1 and L2 caches for each core processor.

A. IBM 370 B. ARM11 MPCore

C. AMD Opteron D. Intel Core i7

11. \_\_\_\_\_\_\_\_\_\_ are characterized by the ability to support thousands of parallel execution threads

A. CPUs B. QPIs

C. GPUs D. ISAs

1. The Intel Core i7-990X chip supports \_\_\_\_\_\_\_\_\_ forms of external communications to other chips.

A. 4 B. 2

C. 6 D. 8

1. The GIC distributes interrupts to individual \_\_\_\_\_\_\_\_\_.

A. dies B. cores

C. QPI D. interconnects

1. The \_\_\_\_\_\_\_\_ feature enables moving dirty data from one CPU to another without writing to L2 and reading the data back in from external memory.

A. migratory lines B. DDI

C. VFP unit D. IPIs

1. The \_\_\_\_\_\_\_\_ is responsible for maintaining coherency among L1 data caches.

A. VFP unit B. distributed interrupt controller

C. snoop control unit (SCU) D. watchdog

**SHORT ANSWER**

1. \_\_\_\_\_\_\_\_\_ states that performance increase is roughly proportional to square root of increase in complexity.
2. \_\_\_\_\_\_\_ law assumes a program in which a fraction (1- *f )*of the execution time involves code that is inherently serial and a fraction *f* that involves code that is infinitely parallelizable with no scheduling overhead.
3. \_\_\_\_\_\_\_\_\_\_ applications are characterized by having a small number of highly threaded processes.
4. \_\_\_\_\_\_\_\_\_ applications are characterized by the presence of many single-threaded processes.
5. \_\_\_\_\_\_\_\_ is a multithreaded process that provides scheduling and memory management for Java applications.
6. \_\_\_\_\_\_\_ is an animation engine used by Valve for its games and licensed for other game developers.
7. \_\_\_\_\_\_\_\_ threading involves the selective use of fine-grain threading for some systems and single threading for other systems.
8. \_\_\_\_\_\_\_\_ threading is when many similar or identical tasks are spread across multiple processors.
9. Individual modules called systems are assigned to individual processors with \_\_\_\_\_\_\_\_ threading.
10. The principal building block of the IBM zEnterprise EC12 mainframe is the \_\_\_\_\_\_\_\_\_\_ .
11. The SCU uses hybrid MESI and \_\_\_\_\_\_\_\_\_ protocols to maintain coherency between the individual L1 data caches and the L2 cache.
12. The most prominent trend in terms of heterogeneous multicore design is the use of both CPUs and \_\_\_\_\_\_\_\_\_\_ on the same chip.
13. From the point of view of an A15 core, an interrupt can be active, inactive, or \_\_\_\_\_\_\_\_\_\_ .
14. A single piece of silicon is called a \_\_\_\_\_\_\_\_.
15. The \_\_\_\_\_\_\_\_\_ is a cache-coherent, point-to-point link based electrical interconnect specification for Intel processors and chipsets that enable high-speed communications among connected processor chips.